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DESCRIPTION

METHOD FOR CONVERTING FRAME, FRAME-CONVERTING CIRCUIT, AND
ELECTRONIC CAMERA

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Technical Field

The present invention relates to electronic cameras that capture and play back moving images, and in particular, relates to methods for converting frames in the National
10 Television System Committee (NTSC) format into those in the Phase Alternation by Line (PAL) format.

Background Art

Many digital still cameras include LCD viewfinders for
15 checking images to be captured and captured images. In addition, many digital still cameras include video output terminals and can display images on, for example, external television receivers.

One type of digital still camera can capture moving
20 images in addition to still images. In most cases, these digital still cameras capture moving images in the video graphics array (VGA) size, i.e., 640 dots in width and 480 dots in height, in the NTSC format in consideration of viewing on personal computers (see Japanese Unexamined
25 Patent Application Publication Nos. 5-122663, 8-172609, and

2001-313896, for example).

In a video camera, i.e., a television camera, a charge coupled device (CCD) image sensor captures an image and outputs image data once every field period, as shown in the upper part of Fig. 6A. The image data is then processed and output from the camera as video signals, as shown in the lower part of Fig. 6A.

In Figs. 6A and 6B, numerals 1, 2, 3, ... are serial numbers assigned to respective certain consecutive frames or fields. A suffix A added to a field number indicates that the field is an odd field, and a suffix B indicates that the field is an even field. A solid arrow indicates image data of an odd field, and a dotted arrow indicates image data of an even field. Hereinafter, the same rules are followed in other drawings.

On the other hand, a digital still camera mainly captures still images and is suitably designed for capturing still images. Thus, in a digital still camera, a CCD image sensor captures an image and outputs image data once every frame period, as shown in the upper part of Fig. 6B. The image data of one frame is split into a first image data component of the odd field, as indicated by a solid arrow, and a second image data component of the even field, as indicated by a dotted arrow. These image data components are output from the camera as video signals, as shown in the

lower part of Fig. 6B.

The above capturing and outputting techniques are also used for capturing moving images. Thus, when a digital still camera captures moving images, the motion of the
5 images is jerky because the interval of capturing images in a digital still camera is twice that in a video camera.

Fig. 7 shows synchronizing frequencies of the NTSC format and the PAL format and the frequency ratio. Thus, when moving images are captured (or are captured and
10 recorded) in the NTSC format, frames of image data in the NTSC format need to be converted into those in the PAL format for viewing on a PAL television receiver.

Figs. 8 and 9 illustrate typical techniques for converting frames. The upper parts of Figs. 8 and 9 show
15 image data before frame conversion. This image data corresponds to, for example, image data that is output from a CCD image sensor or recorded. The lower parts of Figs. 8 and 9 show image data in the PAL format after frame conversion. This image data corresponds to, for example,
20 video signals output from a camera to an external television receiver or video signals supplied to a built-in LCD monitor. In the following description, only frame frequency conversion is described, and the description of horizontal frequency conversion is omitted.

25 In the case of Fig. 8, a first frame to a third frame

in the NTSC format are respectively used for a first frame to a third frame in the PAL format. The odd field in a fourth frame in the NTSC format is used as the odd field 4A in a fourth frame in the PAL format, and the even field is
5 decimated. A fifth frame in the NTSC format is used for the even field 4B in the fourth frame and the odd field 5A in a fifth frame in the PAL format.

After some fields in the NTSC format are decimated, residual fields in the NTSC format are converted into those
10 in the PAL format so that the ratio of frame frequency of the NTSC format to that of the PAL format is eventually 1,200:1,001.

When every 1,200 frames of image data in the NTSC format are decimated to 1,001 frames, the sequence of the
15 decimation is complicated because the location of the field to be decimated shifts as time elapses. Thus, when the decimation is carried out under the control of a central processing unit (CPU), there is a considerable software load.

Thus, the following technique shown in Fig. 9 has been
20 conceived: Each frame of image data is retrieved from, for example, a CCD image sensor or a recording medium every 1/30 seconds, and is converted into that in the PAL format. In this case, the ratio of frame frequency of the input image data to that of the PAL format is as follows:

25 $30 \text{ Hz} : 25 \text{ Hz} = 6 : 5$

Accordingly, as shown in Fig. 9, image data in the PAL format can be obtained by decimating one frame in the NTSC format every six frames, thereby enabling an easy frame conversion.

5 However, in this frame conversion technique, a discontinuous point occurs every five frames in the PAL format, which prevents smooth playback. Moreover, when a digital still camera captures moving images, the motion of the images is jerky as compared with that in a video camera,
10 as described above. Hence, when frames of these moving images are converted with the technique shown in Fig. 9, the motion of the images is jerkier. Moreover, in some cases, an LCD monitor of a digital still camera cannot adapt to the
15 60 Hz synchronizing frequency system and cannot display images.

 The present invention is intended to solve the above problems.

Disclosure of Invention

20 The present invention provides a method for converting frames including:

 retrieving image data of an odd field and image data of an even field, out of moving image data of one first frame period, from a memory to which the moving image data is
25 written, every odd field period and even field period in a

second frame period, respectively;

mixing the retrieved image data of the odd field and
image data of a next odd field that is retrieved next at a
predetermined ratio to output as image data of an odd field
5 in the second frame period;

mixing the retrieved image data of the even field and
image data of a next even field that is retrieved next at a
predetermined ratio to output as image data of an even field
in the second frame period; and

10 changing the mixing ratios for each field in the second
frame period.

Thus, even when original image data is generated every
first frame period, image data of fields in the second frame
period is generated by interpolation. Accordingly, smooth
15 moving images can be displayed based on this generated image
data.

Brief Description of the Drawings

Fig. 1 is a block diagram illustrating an embodiment
20 according to the present invention.

Fig. 2 illustrates the present invention.

Fig. 3 illustrates the present invention.

Fig. 4 is a block diagram illustrating a part of the
present invention.

25 Fig. 5 illustrates the present invention.

Figs. 6A and 6B illustrate the present invention.

Fig. 7 illustrates the present invention.

Fig. 8 illustrates the present invention.

Fig. 9 illustrates the present invention.

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Best Mode for Carrying Out the Invention

(1) Digital still camera

Fig. 1 illustrates a typical digital still camera 10 according to the present invention. An image of an object OBJ is projected onto a CCD image sensor 11 through an imaging lens LNS. Three-primary-color image signals of the object OBJ are output from the CCD image sensor 11. These image signals are supplied to an analog-to-digital (A/D) converter circuit 12 and are A/D-converted to digital image data. This image data is supplied to a camera-signal processing circuit 13, and is converted to image data in the Y-signal, U-signal, and V-signal (YUV) format after processes, for example, white balance correction and gamma correction. The converted image data is written to an area for display in a memory 16 by a memory controller 14 through an image bus 15.

In parallel with this process, the image data is read from the area for display in the memory 16 by the memory controller 14. The read image data is supplied to a display-signal processing circuit 17 through the image bus

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15, and is converted to image data in the red, green, and blue (RGB) format while being D/A-converted to analog image signals. These analog image signals are supplied to an LCD panel 18 and are displayed as color images.

5 In the display-signal processing circuit 17, color video signals in addition to the analog image signals are simultaneously generated. These video signals are output to an external video output terminal 19 to be supplied to a monitoring television receiver (not shown in the drawing).

10 In this process, the resolution of the image data, which is read from the memory 16 and used for display, is converted to, for example, the VGA size by a resolution-converting circuit 21.

15 The image data in the area for display in the memory 16 is also supplied to an image-compressing circuit 22 by the memory controller 14 through the image bus 15 and is compressed into code data in a predetermined format, for example, the Joint Photographic Experts Group (JPEG) format. This code data is written to a work area in the memory 16
20 through the image bus 15. The code data written to the work area in the memory 16 is read by the memory controller 14. This read code data is written to and stored in an external storage medium 24, such as a Memory Stick (trademark registered), by a microcomputer 23.

25 In a playback mode, the code data is read from the

external storage medium 24 by the microcomputer 23 and is written to the work area in the memory 16. This written code data is decompressed into the original image data by the image-compressing circuit 22. This decompressed image data is written to the area for display in the memory 16. This written image data is processed by the display-signal processing circuit 17 to be displayed on the LCD panel 18 as color images and to be output to the external video output terminal 19 as color video signals, as described above.

To smooth the motion of moving images displayed on the LCD panel 18 and moving images of color video signals output to the external video output terminal 19 when these moving images are captured and played back, the following signal processing is carried out in the present invention.

(2) Capturing and playing back moving images

As shown in the upper part of Fig. 2, when moving images are captured, the CCD image sensor 11 is controlled so as to capture an image in the NTSC format and to output image data once every frame period. Thus, as shown in Figs. 6A and 6B, capturing still images can be optimally performed in units of frames as a primary function of a digital still camera.

Moreover, since image capturing is performed in units of frames of the NTSC format in this way, moving images

stored in the external storage medium 24 and moving images read out are also in the NTSC format in units of frames.

(3) Method for converting frames

5 (3-1) Outputting video signals in the NTSC format

In the following description, image data before frame conversion, such as the output of the CCD image sensor 11, is called original image data, and image data and video signals after frame conversion, such as video signals output from a camera, are respectively called output image data and output video signals.

As shown in the upper part of Fig. 2, original image data is obtained in units of frames of the NTSC format. In this case, the original image data is output in the form of video signals in the NTSC format. Thus, the frame frequency of the output video signals is the same as that of the original image data.

Accordingly, the output image data DOUT is a signal component represented by the following expression, as shown in Fig. 2:

$$DOUT = (1 - k)D_n + k \cdot D_{n+1} \cdots (1)$$

where

DOUT is output image data and output video signals after frame conversion,

25 D_n is image data of the odd field or the even field in

the n-th frame in the original image data,

D_{n+1} is image data of the odd field or the even field in the (n+1)-th frame in the original image data, and

k is a predetermined coefficient ($0 \leq k \leq 1$).

5 When the output image data DOUT is that of the odd field, the original image data D_n and D_{n+1} are image data of the odd fields. When the output image data DOUT is that of the even field, the original image data D_n and D_{n+1} are image data of the even fields. According to the field of the
10 output image data DOUT, the coefficient k is changed, for example, as follows:

$k = 1/4$ when the output image data DOUT is that of the odd field, or

$k = 3/4$ when the output image data DOUT is that of the
15 even field.

 That is, two continuous frames of the original image data are mixed for each field at a predetermined ratio that changes every field period to generate the output video signals (the output image data).

20 In this way, even when the original image data is generated every frame period, intermediate image data is generated by interpolation every field period. Displaying based on this generated image data improves the jerkiness when moving images are captured.

(3-2) Outputting video signals in the PAL format

The original image data is obtained as shown in part A of Fig. 3 (part A of Fig. 3 is the same as the upper part of Fig. 2). When this original image data is output as video
5 signals in the PAL format, this original image data is output after a conversion process, as shown in part B of Fig. 3.

That is, in this process, the output image data DOUT is generated according to expression (1). In this process, the
10 coefficient k changes by a predetermined amount every field period of the output image data DOUT according to the shift between frames of the original image data D_n and D_{n+1} and those of the output image data DOUT. Thus, two continuous frames of the original image data are mixed for each field
15 at a predetermined ratio that changes every field period according to the shift between frames of the original image data D_n and D_{n+1} and those of the output image data DOUT to obtain the output video signals.

In Fig. 3, the even field (indicated by a dotted arrow)
20 in the sixth frame of the original image data is used as the even field 4B in the fourth frame of the output image data, and the odd field (indicated by a solid arrow) in the fifth frame of the original image data is used as the odd field 5A in the fifth frame of the output image data. Thus, it seems
25 that the chronological order of the even field 4B in the

fourth frame and the odd field 5A in the fifth frame of the output image data is reversed. However, no problem occurs because of the following reason.

The same original image data is used in the even field 4B in the fourth frame and the odd field 5A in the fifth frame of the output image data, and the odd field and the even field in the original image data include signals generated at the same time. Moreover, the ratio of the fifth frame to the sixth frame of the original image data used in the even field 4B in the fourth frame of the output image data is different from that used in the odd field 5A in the fifth frame. In the even field 4B in the fourth frame of the output image data, the proportion of the fifth frame of the original image data is large, and in the odd field 5A in the fifth frame of the output image data, the proportion of the sixth frame of the original image data is large. Accordingly, the chronological order of the even field 4B in the fourth frame and the odd field 5A in the fifth frame of the output image data is not reversed.

Thus, in the process shown in part B of Fig. 3, even when the original image data is generated every frame period of the NTSC format, image data of each field in the PAL format is generated by interpolation and is displayed. Accordingly, the jerkiness when moving images are captured is improved.

(4) Circuit for generating output image data from original image data

Frames of the original image data are converted to
5 those of the output image data (the output video signals)
mainly by, for example, the memory controller 14 and the
display-signal processing circuit 17, as shown in Fig. 4.
In the main, the case of the output image data in the PAL
format will now be described. The original image data is
10 written to the memory 16 in a bit map corresponding to a
display screen. The original image data is then read from
addresses corresponding to respective horizontal scanning
positions.

As shown in Fig. 7, the total length of 1,200 frame
15 periods of the NTSC format is the same as that of 1,001
frame periods of the PAL format. The NTSC frame is
synchronized with the PAL frame once every total length.

The display-signal processing circuit 17 includes
signal-generating circuits 171 and 172 that generate various
20 types of timing signals. The signal-generating circuit 171
outputs a pulse NTFM every NTSC frame period, as shown in
part D of Fig. 3, as well as a pulse RSTP every 1,200 NTSC
frames, as shown in part C of Fig. 3.

The signal-generating circuit 172 outputs a pulse PAFD
25 and a rectangular-wave signal PFDS every NTSC field period,

or every PAL field period, as shown in part E and part F of Fig. 3. The microcomputer 23 supplies predetermined control signals to the signal-generating circuit 172 to set the period of the pulse PAFD and the period of the signal PFDS to the NTSC field period or the PAL field period. The signal-generating circuit 171 supplies the pulse RSTP to the signal-generating circuit 172.

Since the original image data is read from addresses of the memory 16, corresponding to respective horizontal scanning positions, the memory controller 14 includes a group of registers (latch circuits) 141 to 143, a group of registers (latch circuits) 144 to 146, an adding circuit 147, and a data selector 148. The registers 141 to 143 set an odd-field start address ODST (the start address of the first odd line) in an address counter (not shown in the drawing) in the memory 16, and the registers 144 to 146 store data ADNO indicating the number of addresses (the number of pixels) per line.

The memory 16 includes the address counter, which is not shown in the drawing. When a start address is supplied, a readout address is incremented every odd line or even line, starting from the start address, and image data of an odd field or an even field is sequentially read out.

When the microcomputer 23 supplies the odd-field start address ODST and a clock CK to the register 141, which

stores the start address ODSF. An output from the register 141 and the pulse NTFM from the signal-generating circuit 171 are supplied to the register 142, which stores the odd-field start address ODSF. An output from the register 142
5 and the pulse PAFD from the signal-generating circuit 172 are supplied to the register 143, which outputs the odd-field start address ODSF every pulse PAFD.

Similarly, the microcomputer 23 supplies the data ADNO indicating the number of addresses per line to the register
10 144, and the data ADNO is output from the register 146.

The adding circuit 147 adds the odd-field start address ODSF from the register 143 to the data ADNO, indicating the number of addresses per line, from the register 146. Thus, the adding circuit 147 outputs an even-field start address
15 EVSF (the start address of the first even line).

The odd-field start address ODSF, the even-field start address EVSF, and the signal PFDS serving as a control signal from the signal-generating circuit 172 are supplied to the data selector 148 (in this case, the signal PFDS
20 inverts every PAL field period). Thus, as shown in part G of Fig. 3, the data selector 148 alternately outputs the odd-field start address ODSF and the even-field start address EVSF every PAL field period.

These start addresses output from the data selector 148
25 are supplied to the memory 16. Thus, the original image

data is retrieved from the memory 16 every PAL field period.

The retrieved original image data is supplied to an interpolating circuit 76 provided in the display-signal processing circuit 17. The interpolating circuit 76

5 converts the original image data in the memory 16 to the output image data by interpolation according to expression (1), and includes a converting circuit 176 and arithmetic circuits (a subtracting circuit 177, a multiplying circuit 178, and an adding circuit 179). The converting circuit 176
10 synchronously outputs image data D_n of the odd field or the even field in the n -th frame and image data D_{n+1} of the odd field or the even field in the $(n+1)$ -th frame, out of the original image data read from the memory 16.

The image data D_n and D_{n+1} output from the converting
15 circuit 176 are supplied to the subtracting circuit 177, which subtracts the data D_n from the data D_{n+1} and supplies the result $(D_{n+1} - D_n)$ to the multiplying circuit 178. The coefficient k is also supplied to the multiplying circuit 178 from a coefficient-generating circuit 73, described
20 below, to be multiplied by the value $(D_{n+1} - D_n)$. The result $k(D_{n+1} - D_n)$ and the data D_n from the converting circuit 176 are supplied to the adding circuit 179.

The adding circuit 179 outputs the image data DOUT represented by the following expression:

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$$k(D_{n+1} - D_n) + D_n = (1 - k)D_n + k \cdot D_{n+1}$$

• • • (2)

5 on a monitoring television receiver connected to the
external video output terminal 19.

10 generating circuit 73 generates the coefficient k, which
changes according to the shift between the NTSC frame and
the PAL frame, as described above.

15 resolution of the output image data is 1/128 of the field
period of the PAL format.

20 changes the initial value and the delta value, an adding
circuit 174 for accumulation, and a 7-bit register (a latch
circuit) 175 that stores the accumulated value. The
microcomputer 23 outputs, for example, "0" and "76" as the
initial value and the delta value, respectively, to the data
25 selector 173 and the adding circuit 174. The signal-

generating circuit 171 outputs the pulse RSTP to the data selector 173 as a control signal.

When RSTP = 1, the initial value "0" is output from the data selector 173 and the register 175 stores the output
5 initial value "0" upon receiving the pulse PAFD from the signal-generating circuit 172. Thus, as shown in part H of Fig. 3, an output Qk from the register 175 is "0" for one field period (one PAL field period) after the pulse RSTP is sent. Simultaneously, the output Qk (= 0) from the register
10 175 and the delta value "76" from the microcomputer 23 are summed up in the adding circuit 174, and the summed-up value "76" is output from the adding circuit 174.

Subsequently, the value of RSTP is "0". When one field period (the period of the field 1A) has elapsed since the
15 value of RSTP is "0", RSTP = "0". Thus, the current value "76" of the output from the adding circuit 174 is supplied to the register 175 through the data selector 173, and the register 175 stores the value "76" upon receiving the pulse PFDS. As shown in part H of Fig. 3, Qk = 76 from this point
20 of time. Accordingly, the output from the adding circuit 174 is "152".

When a further field period of the PAL format has elapsed, the output "152" from the adding circuit 174 is supplied to the register 175 through the data selector 173
25 and the register 175 stores the value "152" upon receiving

the pulse PFDS. However, since the register 175 is a 7-bit register, only the lower 7 bits of the output "152" from the adding circuit 174 are latched into the register 175. As shown in part H of Fig. 3, the output Q_k from the register 175 is "24" ($= 152 - 128$).

The above operation is repeated every field period of the PAL format, so that the output Q_k from the register 175 changes every field period of the PAL format, as shown in part H of Fig. 3. This output Q_k is shifted toward the least significant bit (LSB) by seven bits to be supplied to the multiplying circuit 178 as the coefficient k . That is, the value $Q_k/128$ is supplied to the multiplying circuit 178 as the coefficient k . Multiplying both sides of expression (1) by 128 results in:

$$\begin{aligned} 128 \times \text{DOUT} &= 128 \times (1 - k)D_n + 128 \times k \times D_{n+1} \\ &= (128 - Q_k)D_n + Q_k \cdot D_{n+1} \quad \dots (3) \end{aligned}$$

Thus, in Fig. 3, since $Q_k = 0$ ($k = 0$) for the period of the odd field 1A in the first frame of the output image data, image data of the odd field 1A is generated by mixing the odd field in the first frame and the odd field in the second frame of the original image data in the ratio of 128:0, as shown in part I of Fig. 3. Since $Q_k = 76$ ($k = 76/128$) for the period of the even field 1B in the first frame of the output image data, image data of the even field 1B is generated by mixing the even field in the first frame and

the even field in the second frame of the original image data in the ratio of 52:76.

Furthermore, since $Q_k = 24$ ($k = 24/128$) for the period of the odd field 2A in the second frame of the output image data, image data of the odd field 2A is generated by mixing
5 the odd field in the second frame and the odd field in the third frame of the original image data in the ratio of 104:24. Since $Q_k = 100$ ($k = 100/128$) for the period of the even field 2B in the second frame of the output image data,
10 image data of the even field 2B is generated by mixing the even field in the second frame and the even field in the third frame of the original image data in the ratio of 28:100.

Continuously, image data of fields of two continuous
15 frames of the original image data are mixed at a certain ratio shown in part I of Fig. 3 every field period of the PAL format to generate the output image data DOUT (the output video signals) in the same way.

Thus, even when the original image data is generated
20 every frame period of the NTSC format, image data of each field in the PAL format is generated by interpolation. Since this generated image data is the output image data DOUT, the jerkiness when moving images are captured is improved to smooth the motion of the moving images.

25 On the other hand, when the output image data DOUT in

the NTSC format is generated, the microcomputer 23 controls the signal-generating circuit 172 so as to set the period of the pulse PAFD and the period of the signal PFDS to the NTSC field period. The microcomputer 23 outputs, for example,
5 "32" and "64" as the initial value and the delta value, respectively, to the data selector 173 and the adding circuit 174.

In this case, since the output Q_k from the coefficient-generating circuit 73 alternately changes to "32" or "96"
10 every field period of the NTSC format, the coefficient k , which is the mixing ratio in the interpolating circuit 76, alternately changes to $1/4$ or $3/4$ every field period of the NTSC format. Thus, the process is as shown in Fig. 2, so that smooth moving images can be displayed when the output
15 image data DOUT in the NTSC format is generated.

(5) Another type of interpolating circuit 76

Fig. 5 illustrates another type of the interpolating circuit 76. In this case, the image data D_n and D_{n+1} output
20 from the converting circuit 176 and coefficients $(1-k)$ and k output from the coefficient-generating circuit 73 are supplied to multiplying circuits 271 and 272. Then, the results of multiplication from the multiplying circuits 271 and 272 are supplied to the adding circuit 179, which
25 outputs the image data DOUT represented by expression (1).

According to the present invention, even when the original image data is generated every frame period of the NTSC format, image data of fields in the PAL format is generated by interpolation to be used for display. Thus,
5 smooth moving image can be displayed.